

What is claimed is:

- Sub  
a1
1. An interface circuit, comprising:  
a digital signal processor (DSP);  
a data access arrangement (DAA); and  
a charge pump, coupled between said DSP and said DAA, said  
charge pump providing operating power to said DAA. /
2. An interface circuit as set forth in claim 1, wherein  
said charge pump comprises:  
a first capacitive element having an input side connected to  
said DSP and an output side connected to said DAA;  
a second capacitive element having an input and an output  
each connected to said DAA; and  
a rectifying element coupled between the output side of said  
first capacitive element and said second capacitive element.
3. An interface circuit as set forth in claim 2, wherein  
said DSP includes a clock generator generating first and second  
clock pulses out of phase with each other by 180° and wherein  
said first capacitive element comprises:  
a first capacitor coupled to receive said first clock pulse;  
and  
a second capacitor coupled to receive said second clock  
pulse, wherein said first capacitive element continuously outputs  
a positive output voltage to said rectifying element.

4. An interface circuit as set forth in claim 3, wherein said rectifying element comprises a diode rectifier.

5. An interface circuit as set forth in claim 4, wherein said DAA includes a clock regeneration element connected in parallel with said rectifying circuit to remove DC level shift and regenerate a clock pulse for use by the DAA which is essentially identical to the clock pulse output by said clock generator.

6. An interface circuit as set forth in claim 5, wherein said second capacitive element comprises a storage capacitor which stores the charge transferred by said first and said second capacitors.

7. A method of providing power to a data access arrangement (DAA) in an interface circuit of a telecommunication network when a telephone line connected to said interface circuit is in the on-hook state, said interface circuit including a digital signal processor (DSP) having a clock generator, said method comprising the steps of:

inserting a charge pump between said DSP and said DAA;

generating a power signal across said charge pump by inputting the output of said clock generator to said charge pump; and

storing said generated power signal for use by said interface.

8. An interface circuit, comprising:

a driver circuit for developing a charge across capacitive elements of said interface circuit;

a data access arrangement (DAA); and

a charge pump, coupled between said DSP and said driver circuit, said charge pump providing operating power to said DAA.

9. An interface circuit as set forth in claim 8, wherein said charge pump comprises:

a first capacitive element having an input side connected to said driver circuit and an output side connected to said DAA;

a second capacitive element having an input and an output each connected to said DAA; and

a rectifying element coupled between the output side of said first capacitive element and said second capacitive element.

10. An interface circuit as set forth in claim 9, wherein said driver circuit comprises a clock generator generating first and second clock pulses out of phase with each other by 180° and wherein said first capacitive element comprises:

a first capacitor coupled to receive said first clock pulse; and

a second capacitor coupled to receive said second clock pulse, wherein said first capacitive element continuously outputs a positive output voltage to said rectifying element.

11. An interface circuit as set forth in claim 10, wherein  
5 said rectifying element comprises a diode rectifier.

12. An interface circuit as set forth in claim 11, wherein  
said DAA includes a clock regeneration element connected in  
parallel with said rectifying circuit to remove DC level shift  
and regenerate a clock pulse for use by the DAA which is  
10 essentially identical to the clock pulse output by said clock  
generator.

13. An interface circuit as set forth in claim 12, wherein  
said second capacitive element comprises a storage capacitor  
which stores the charge transferred by said first and said second  
15 capacitors.

09192651.11699  
86977" T5926T60

add a3